otherwise alter deposition conditions for different reaction chambers and for different selected conditions to achieve saturated, self-terminating phases at acceptable deposition rates.

Please replace the paragraph beginning on page 37, line 12 with the following replacement paragraph:

At the same time, high step coverage provided by the methods disclosed herein enable formation of the desired thickness uniformly over all surfaces of the HSG layer, including top, sidewall, reentrant and neck region surfaces. Accordingly, the dielectric layer 302 over the HSG silicon layer 304 has a minimum thickness that is preferably greater than about 95%, and more preferably greater than about 98% of its maximum thickness at any point of the structure and at any point during the process.

Remarks

In the Advisory Action, the Examiner maintained the rejection of Claims 1-35 and 55-66 under 35 U.S.C. § 103 as being obvious over Wu (U.S. Patent No. 5,650,351) in view of Suntola et al. (U.S. Patent No. 4,058,430). Dependent claims were found to be obvious over several additional secondary references.

The foregoing amendments were made in order to clarify the invention. They are fully supported by the specification and claims as originally filed and do not add new matter. Support for the amendments can be found throughout the specification, at least at page 21, lines 23-26 and in original claim 36. Attached hereto is a marked-up version of the changes made by the current amendments. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Claim rejections under 35 U.S.C. §103

In an obviousness rejection under 35 U.S.C. §103, motivation to combine the references must be shown. As explained by the Federal Circuit in In re Lee, "the examiner can satisfy the burden of showing obviousness of the combination '**only** by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.'" 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002), citing In re Fitch 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992), emphasis added. Here, the Examiner has provided no specific, objective suggestion to combine the references,

stating only that "it would be obvious to combine the references since the ALD deposition is well known in the art." Thus, the Examiner relies on the common knowledge of one of ordinary skill in the art.

Even in such a case, "**particular findings** must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have **selected these components** for combination in the manner claimed." Id. at 1433, citing In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000), emphasis added. Here, the Examiner has made no particular findings and thus has not met his burden in making a §103 rejection.

The Examiner found that the references of record showing the incompatibility of high k materials and HSG silicon are immaterial because Wu teaches a high k material over silicon, stating "it is not necessary to consider references that teach the incompatibility of silicon and high k materials." However, the Examiner could not make the **required particular findings** without considering all of the evidence of record. As stated by the Federal Circuit:

> In determining whether such a suggestion can fairly be gleaned from the prior art, ***the full field of the invention must be considered*** for the person of ordinary skill is charged with knowledge of the entire body of technological literature, including that which might ***lead away*** from the claimed invention.

In re Dow Chemical Co., 5 U.S.P.Q.2d at 1531-32 (emphasis added).

Applicants respectfully submit that the Examiner's position is contrary to the position taken by the Federal Circuit, and that in making an obviousness rejection the Examiner **must** consider all of the relevant evidence of record, including that which teaches away from the claimed invention.

With respect to the present application, the evidence of record overwhelmingly shows that the incompatibility of polysilicon and high k materials was well accepted in the art at the time of the invention. Further, the evidence shows that the industry responded to this incompatibility by switching from silicon to metal electrodes. The single line of throwaway disclosure in the Wu reference regarding high k materials and HSG silicon does nothing to counter the understanding that high k materials and silicon are incompatible.

The recognition of this incompatibility and the accepted solution was detailed in Applicants' Response to Final Office Action, filed November 13, 2001, which is hereby incorporated by reference. In addition to the references already of record, Applicants submit

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herewith a Supplemental Information Disclosure Statement identifying a number of additional references that reflect recognition in the art of the incompatibility of polysilicon and high k materials and the accepted approach for dealing with this incompatibility. For example, U.S. patent no. 5,633,781 describes a capacitor which intentionally avoids the combination of silicon and a high dielectric material (column 2, lines 7-10) and explicitly states that "high dielectric constant materials **must be isolated from silicon**" (column 1, lines 65-66). Similarly, U.S. patent no. 5,392,189 states that "Unfortunately, high dielectric constant materials are incompatible with existing processes..." (column 1, lines 53-55). U.S. patent nos. 5,187,638, 5,617,290 and 5,619,393 also teach away from the combination of high k material and polysilicon.

Thus, Applicants submit that the knowledge generally available to one of ordinary skill in the art would **not** "lead that individual to combine the references." Id., supra. In particular, one of ordinary skill in the art would **not** be motivated to choose the Wu reference, in view of all of the references teaching incompatibility of high k materials and polysilicon, for combination in the manner claimed by the Examiner. Thus Applicants request that this rejection be withdrawn.

Conclusion

For the reasons presented above, Applicants respectfully submit that all pending claims are in condition for allowance, and an early action to that effect is respectfully solicited. If any issues remain or require further clarification, the Examiner is respectfully requested to call Applicants' counsel at the number listed below in order to resolve such issues promptly.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: March 8, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning on page 21, line 21 has been amended as follows:

Note that the parameters in the tables below are exemplary only. Each process phase is desirably arranged to saturate the bottom electrode surfaces. Purge steps are arranged to remove reactants between reactive phases from the reaction chamber. The illustrative ALD processes achieve better than about 95% thickness uniformity, and more preferably greater than about 98% thickness uniformity over HSG grains with average gain sizes of about 400 Å. Thickness uniformity, as used herein, is defined as the ~~percentage of a~~ thickness minimum as a percentage of the thickness maximum. In view of the disclosure herein, the skilled artisan can readily modify, substitute or otherwise alter deposition conditions for different reaction chambers and for different selected conditions to achieve saturated, self-terminating phases at acceptable deposition rates.

The paragraph beginning on page 37, line 12 has been amended as follows:

At the same time, high step coverage provided by the methods disclosed herein enable formation of the desired thickness uniformly over all surfaces of the HSG layer, including top, sidewall, reentrant and neck region surfaces. Accordingly, the dielectric layer 302 over the HSG silicon layer 304 has a minimum thickness that is preferably ~~no more~~ greater than about 95%, and more preferably ~~no more~~ greater than about 98% of its maximum thickness at any point of the structure and at any point during the process.

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